Figure 1

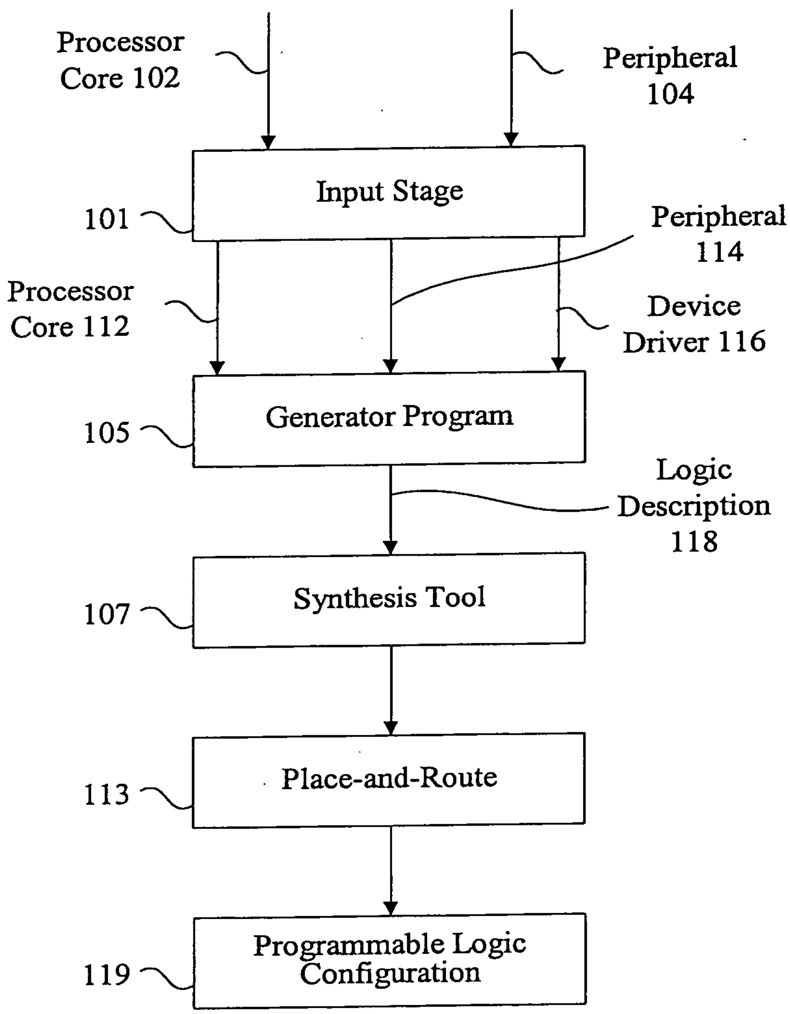


Figure 2

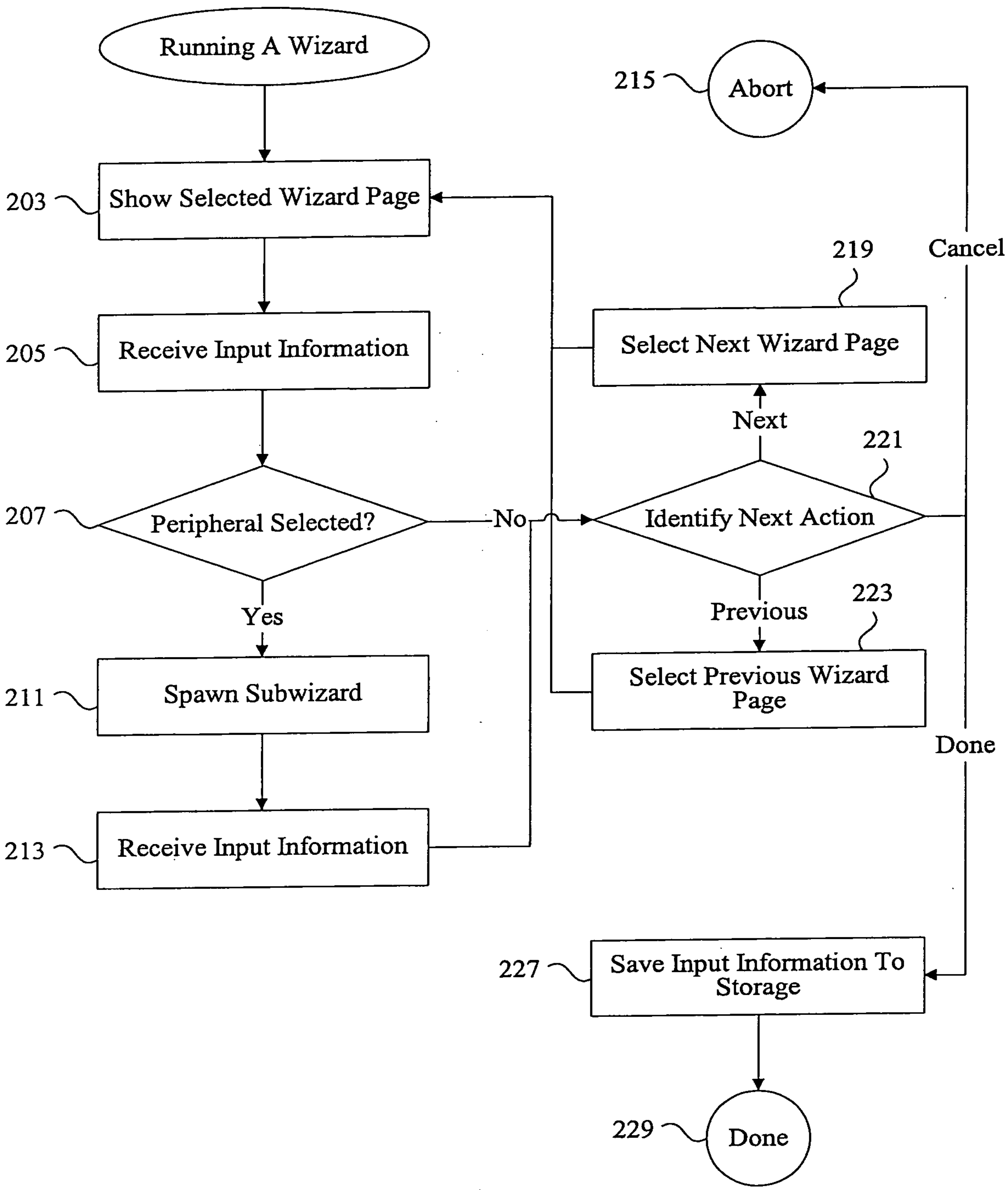
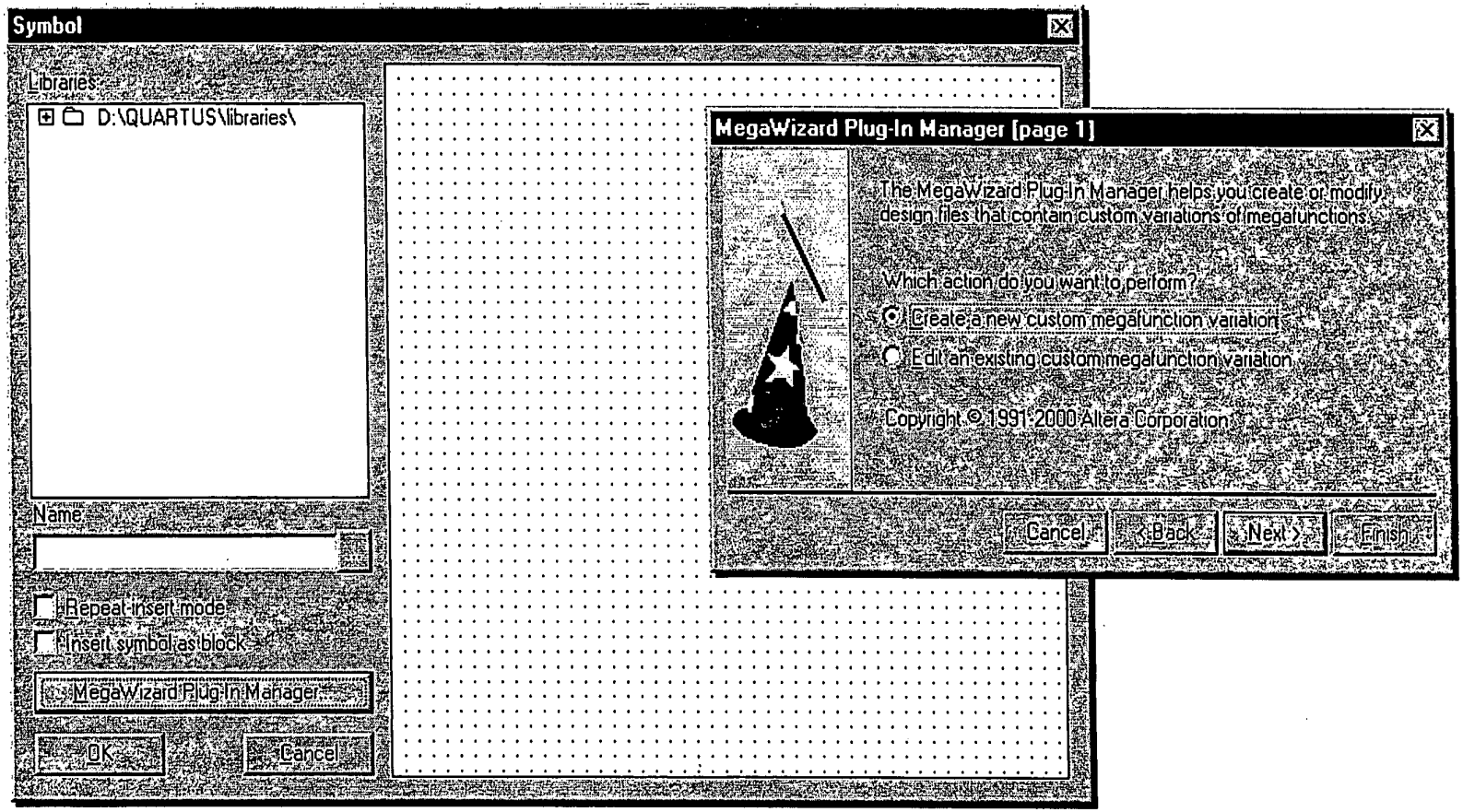


FIGURE 3A



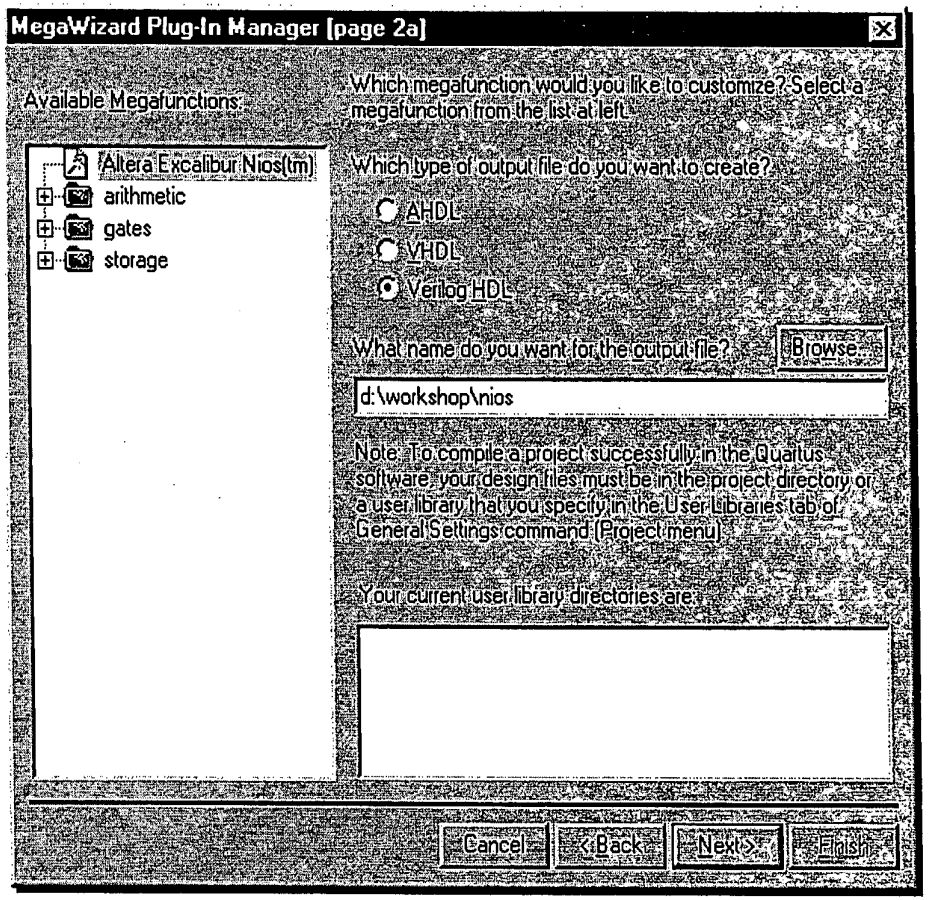


FIGURE 3B

FIGURE 3C

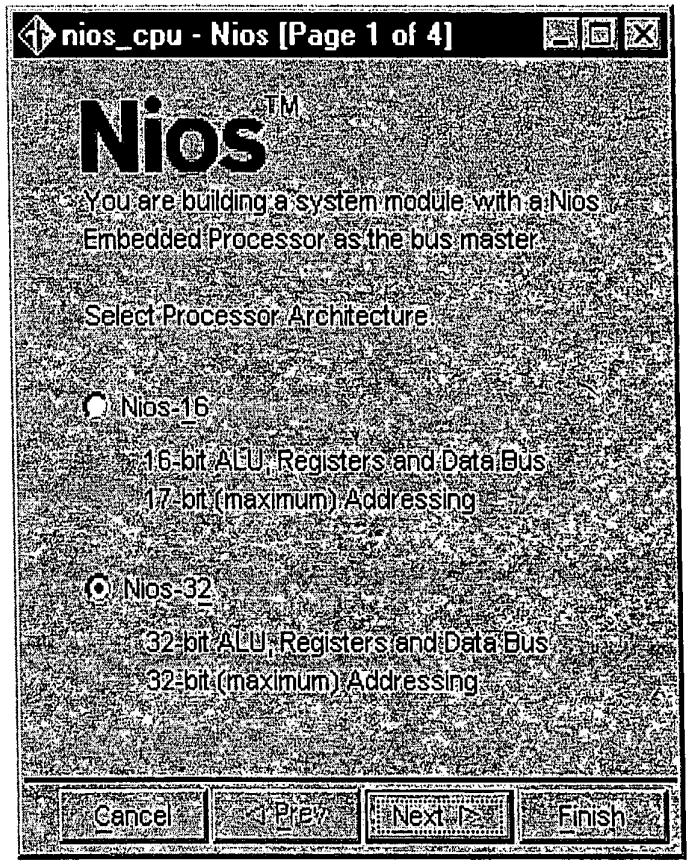


FIGURE 3D

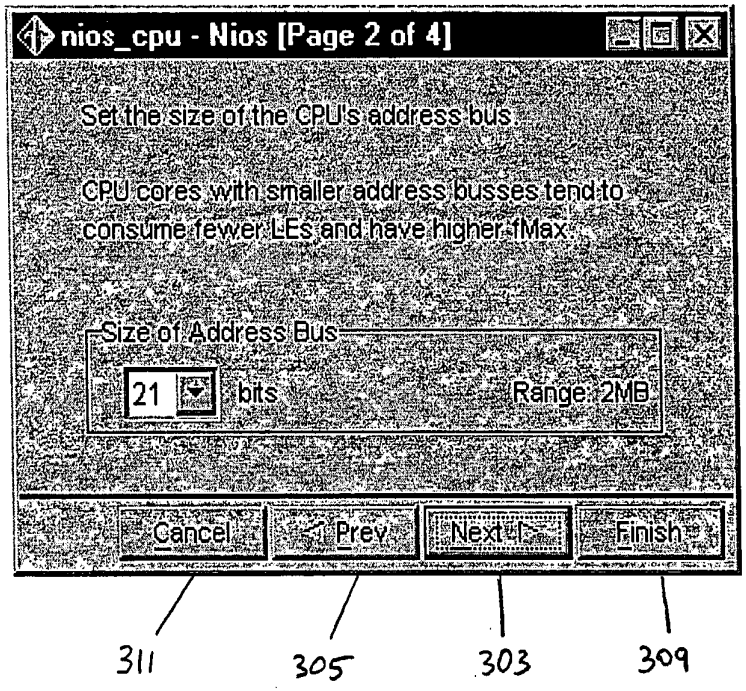

nios_cpu - Nios [Page 2 of 4]
Set the size of the CPU's address bus
CPU cores with smaller address busses tend to consume fewer LEs and have higher fMax.
Size of Address Bus
21
bits
Range: 2MB
Cancel
< Prev
Next >
Finish
311
305
303
309

FIGURE 3E

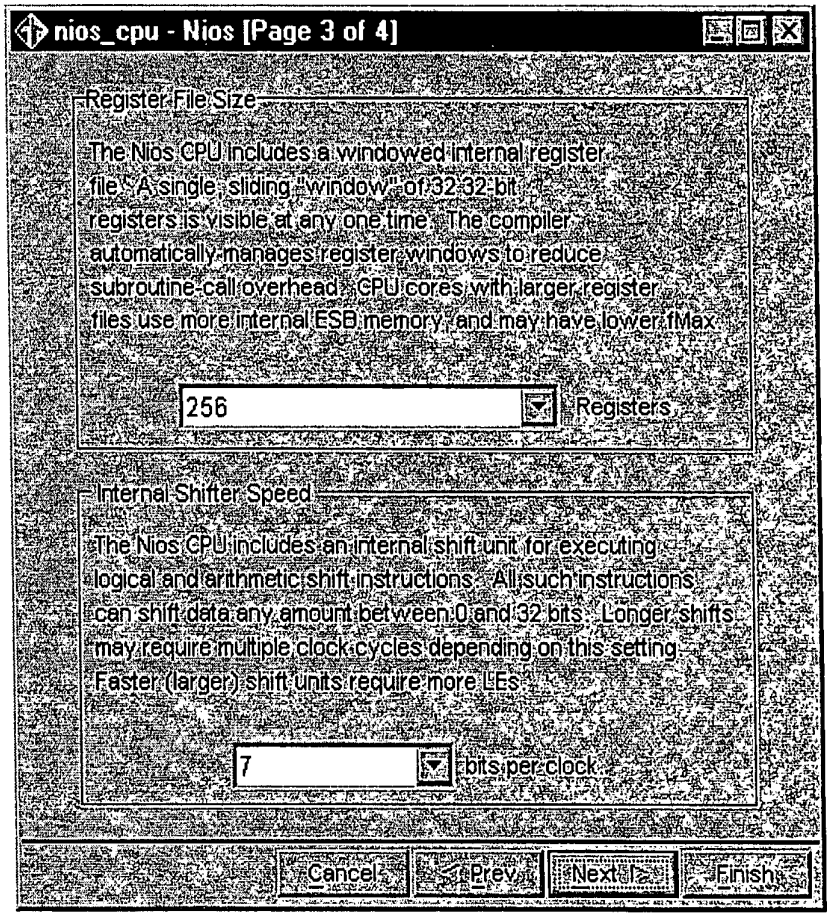


FIGURE 3F

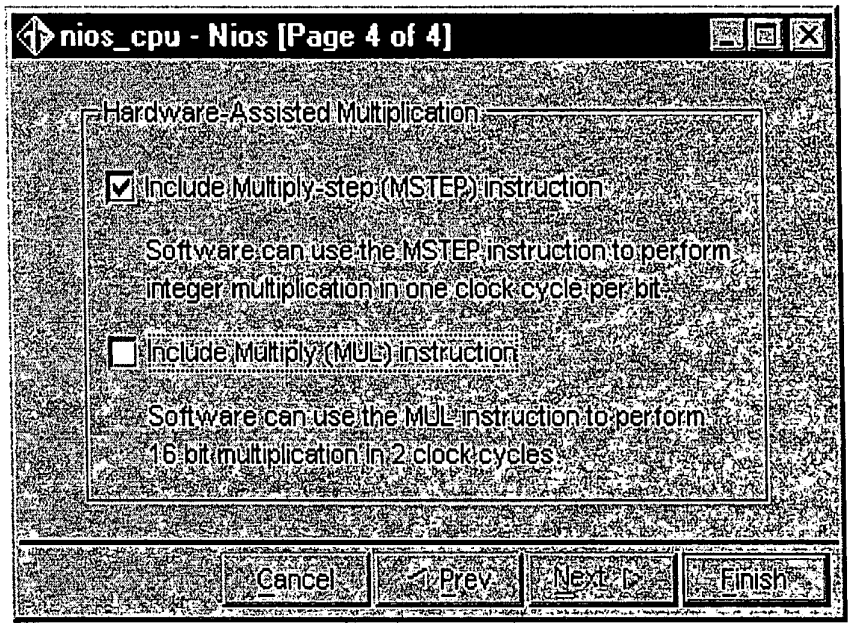


FIGURE 3G

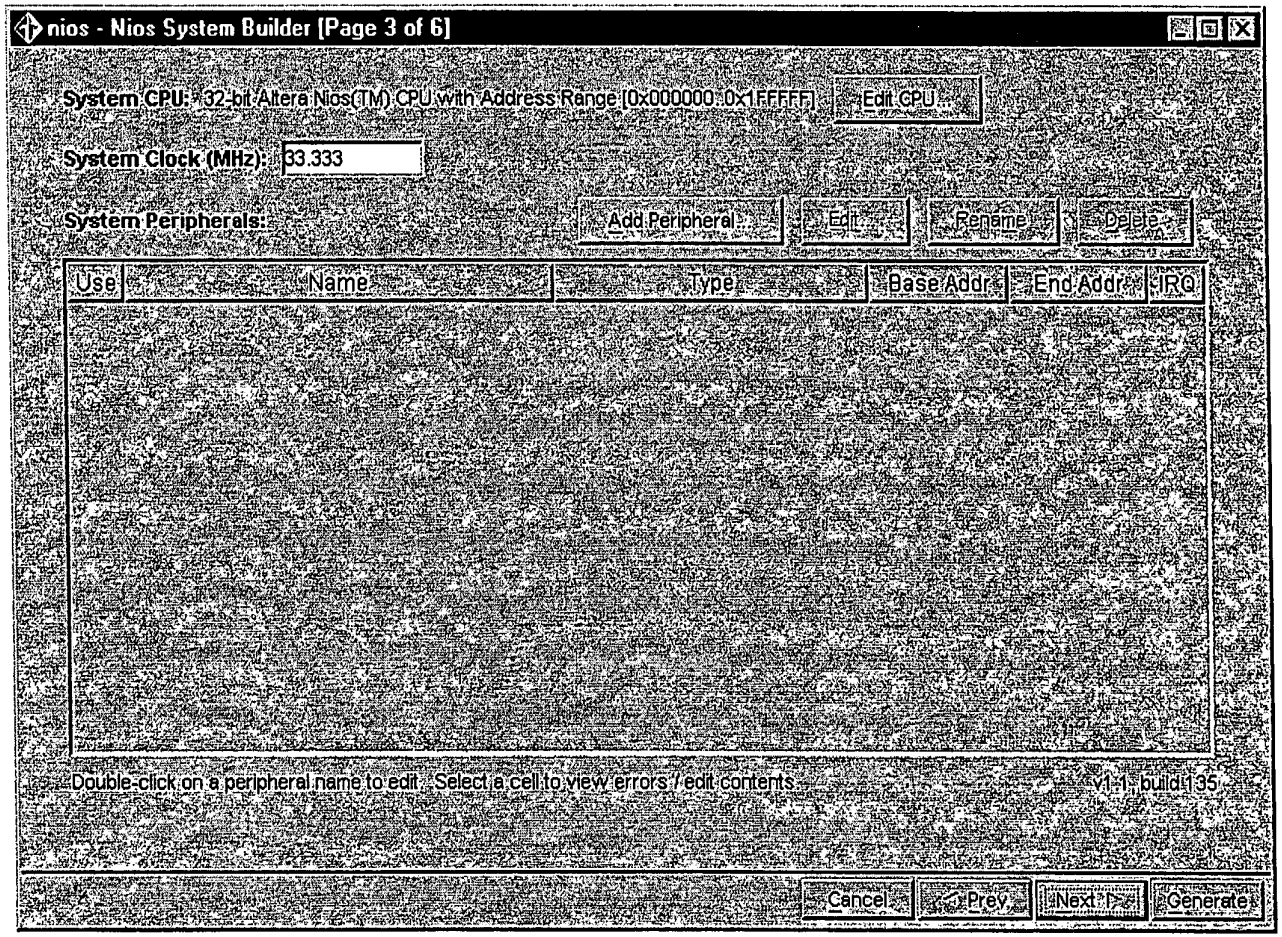


FIGURE 3H

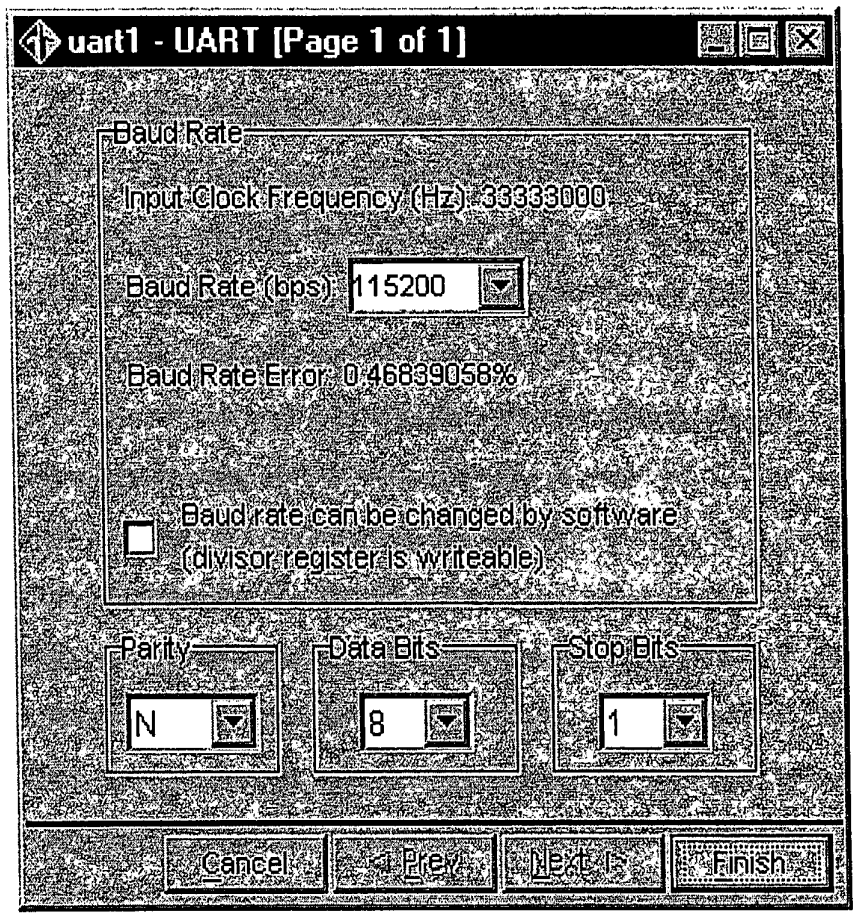

uart1 - UART [Page 1 of 1]
Baud Rate
Input Clock Frequency (Hz) 33333000
Baud Rate (bps) 115200
Baud Rate Error 0.46839058%
Baud rate can be changed by software
(divisor register is writeable)
Parity
N
Data Bits
8
Stop Bits
1
Cancel
< Prev
Next >
Finish

FIGURE 3I

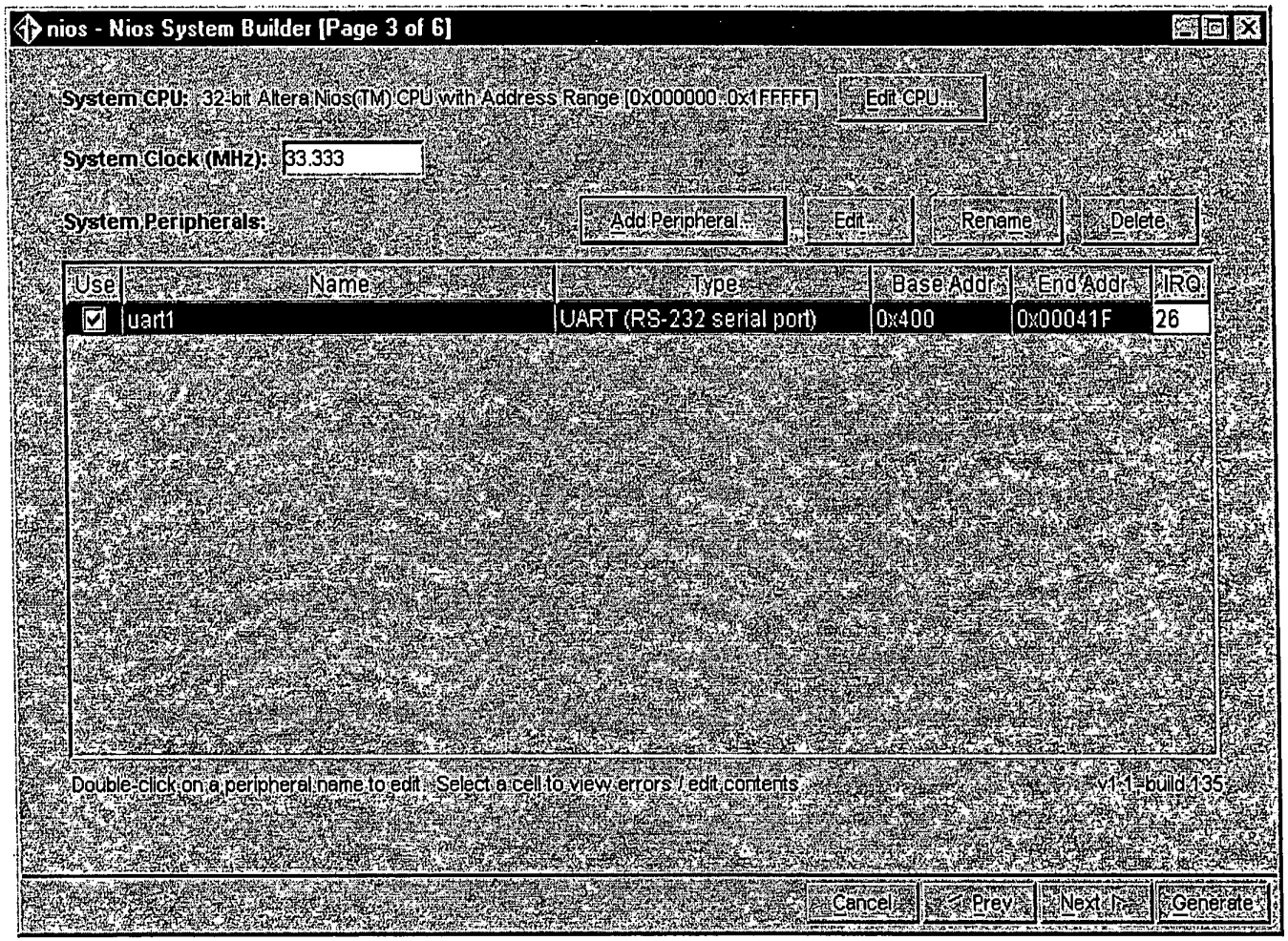

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename
Delete
Use
Name
Type
Base Addr.
End Addr.
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
Double-click on a peripheral name to edit. Select a cell to view errors / edit contents.
v1.1 build 135
Cancel
< Prev
Next >
Generate

FIGURE 3J

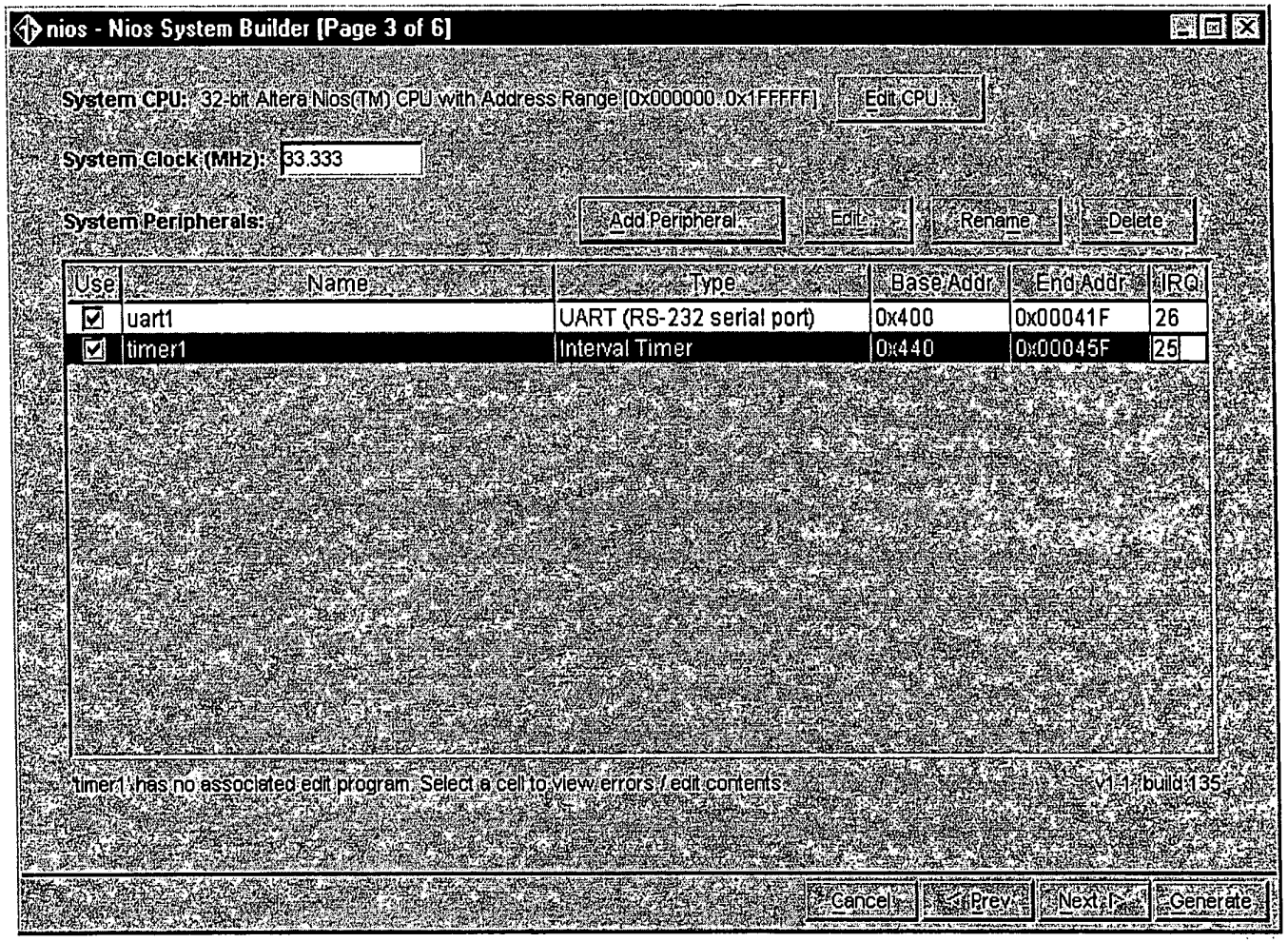

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename...
Delete
Use
Name
Type
Base Addr.
End Addr.
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
timer1
Interval Timer
0x440
0x00045F
25
timer1 has no associated edit program. Select a cell to view errors / edit contents.
v1.1 build 135
Cancel
< Prev
Next >
Generate

FIGURE 3K

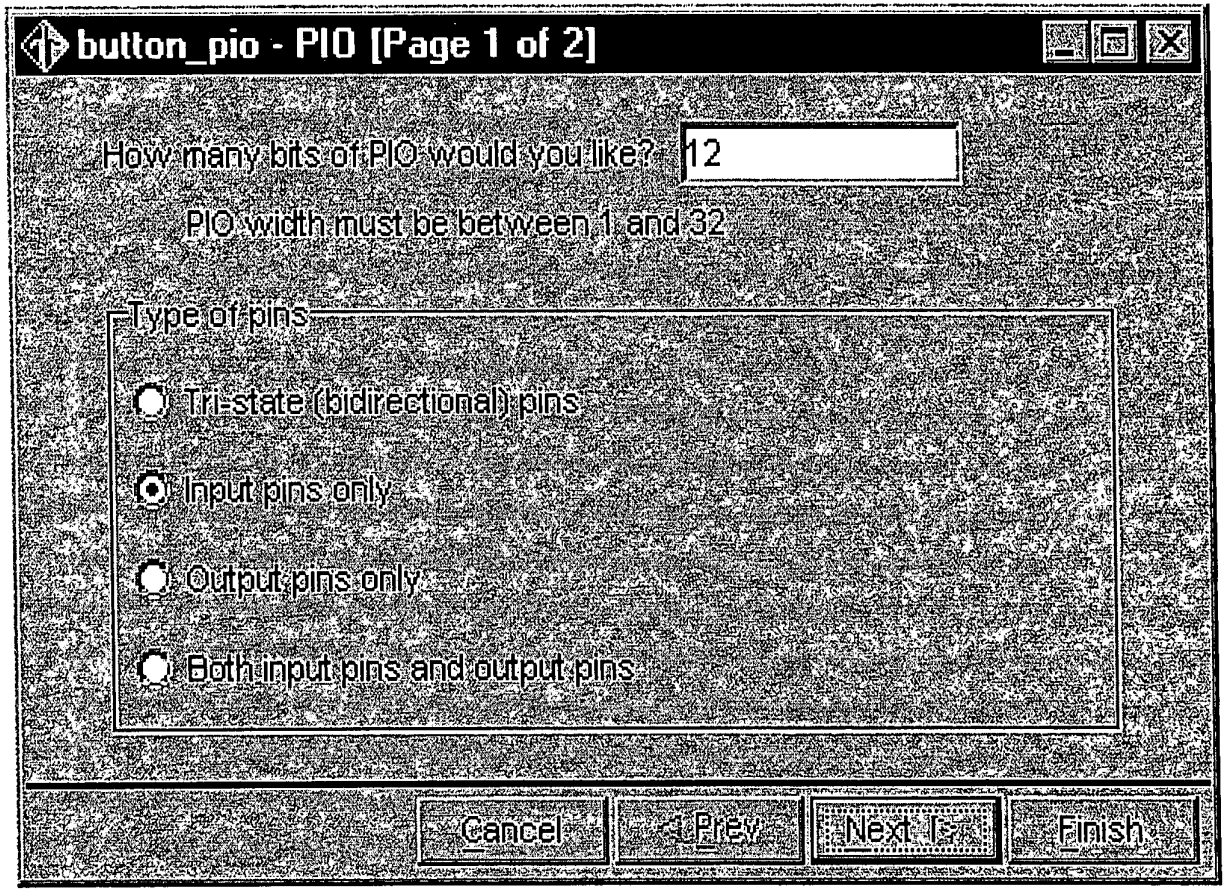

button_pio - PIO [Page 1 of 2]
How many bits of PIO would you like?
12
PIO width must be between 1 and 32
Type of pins
Tri-state (bidirectional) pins
Input pins only
Output pins only
Both input pins and output pins
Cancel
< Prev
Next >
Finish

FIGURE 3L

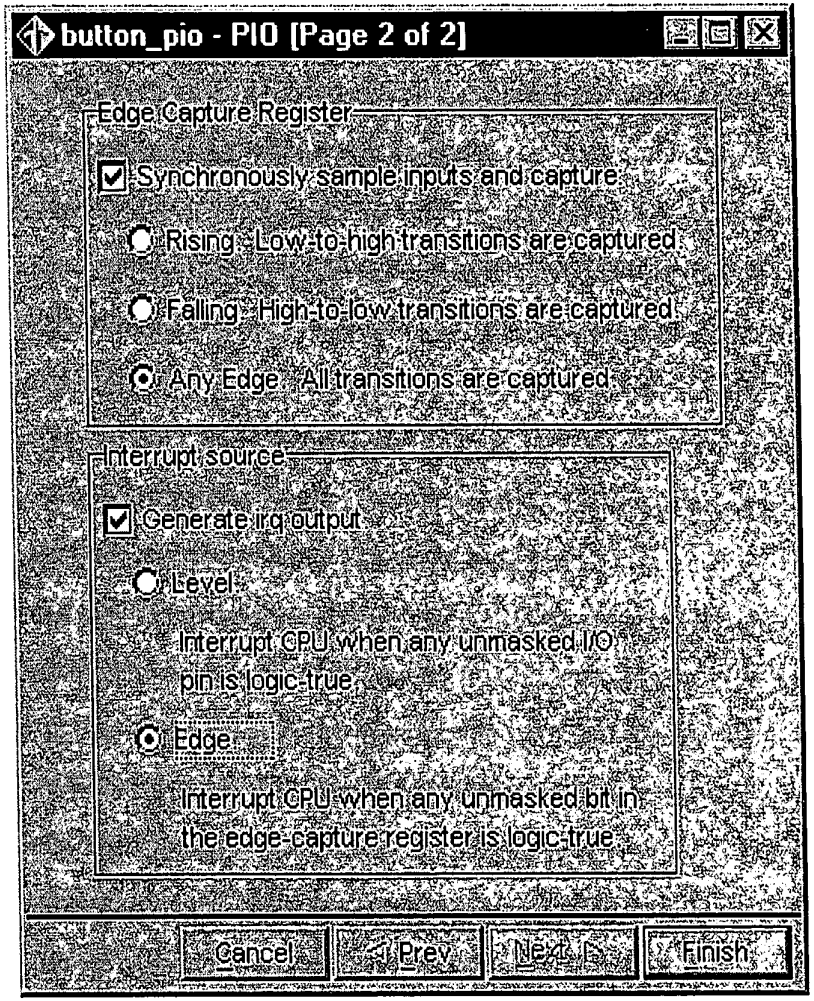


FIGURE 3M

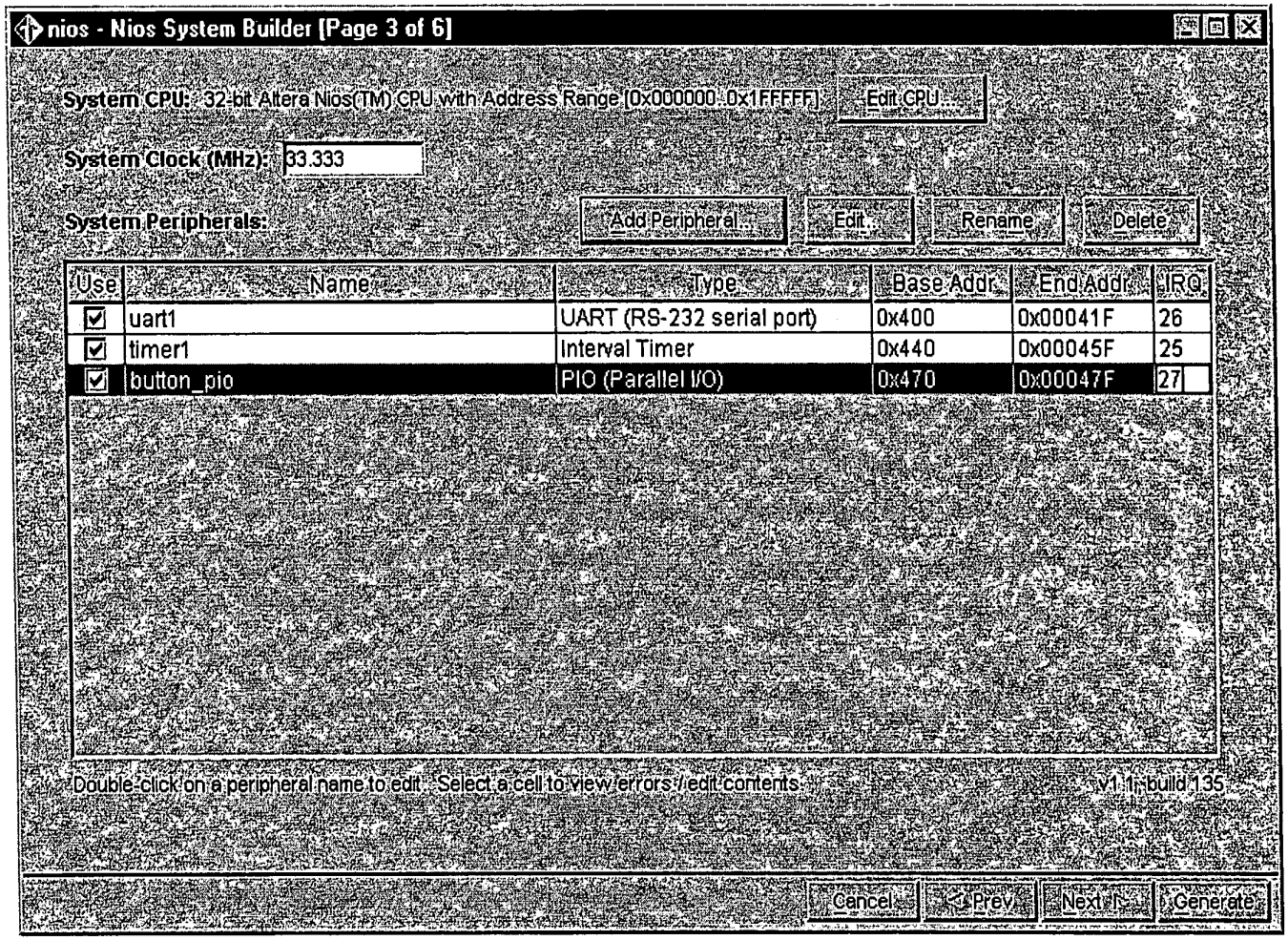
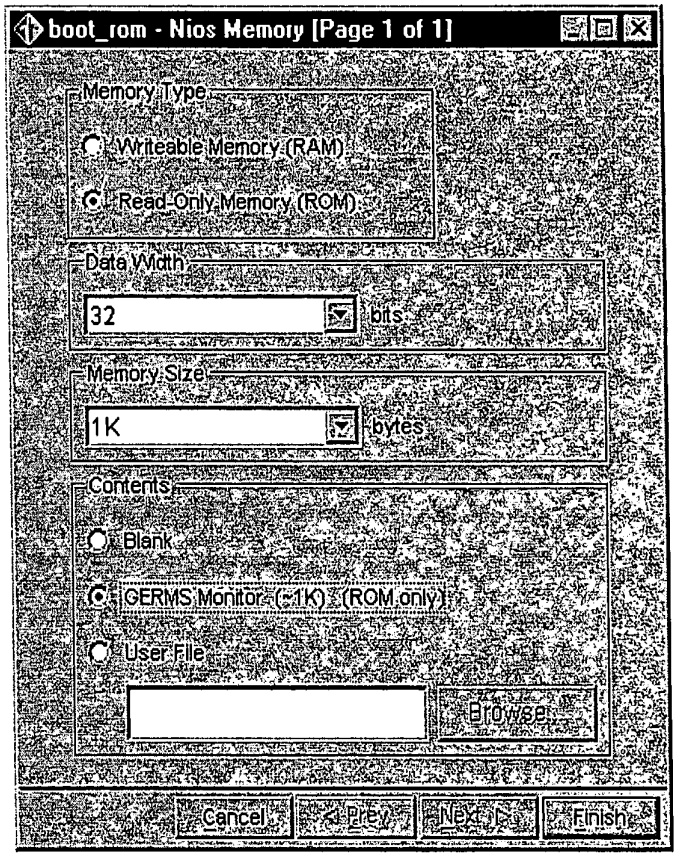

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename
Delete
Use
Name
Type
Base Addr.
End Addr.
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
timer1
Interval Timer
0x440
0x00045F
25
button_pio
PIO (Parallel I/O)
0x470
0x00047F
27
Double-click on a peripheral name to edit. Select a cell to view errors / edit contents.
v1.1 build 135
Cancel
Prev
Next
Generate

FIGURE 3N



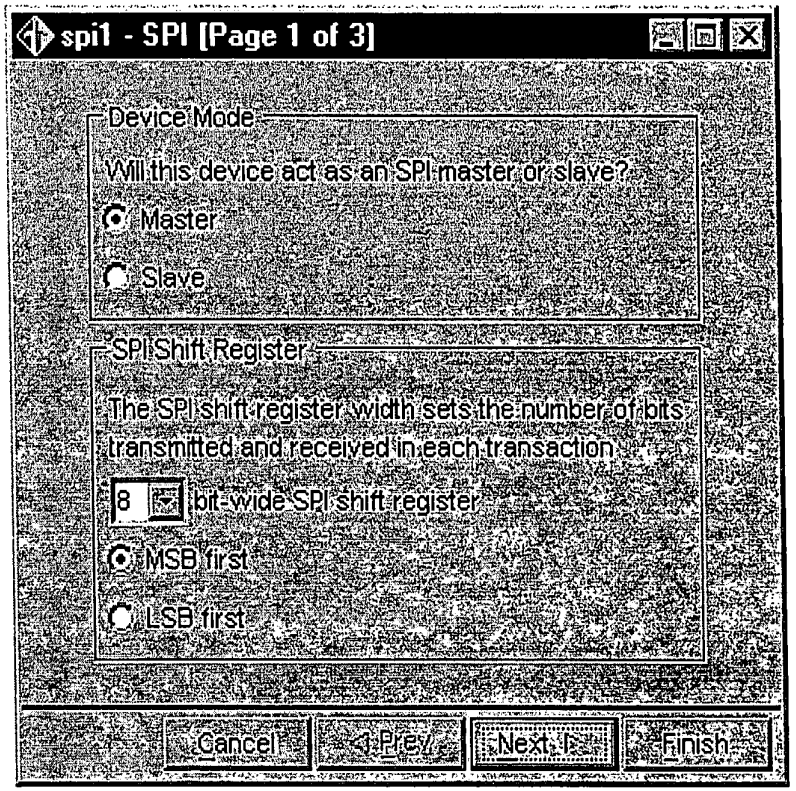

spi1 - SPI [Page 1 of 3]
Device Mode
Will this device act as an SPI master or slave?
Master
Slave
SPI Shift Register
The SPI shift register width sets the number of bits transmitted and received in each transaction.
8
bit-wide SPI shift register
MSB first
LSB first
Cancel
< Prev
Next >
Finish

FIGURE 3O

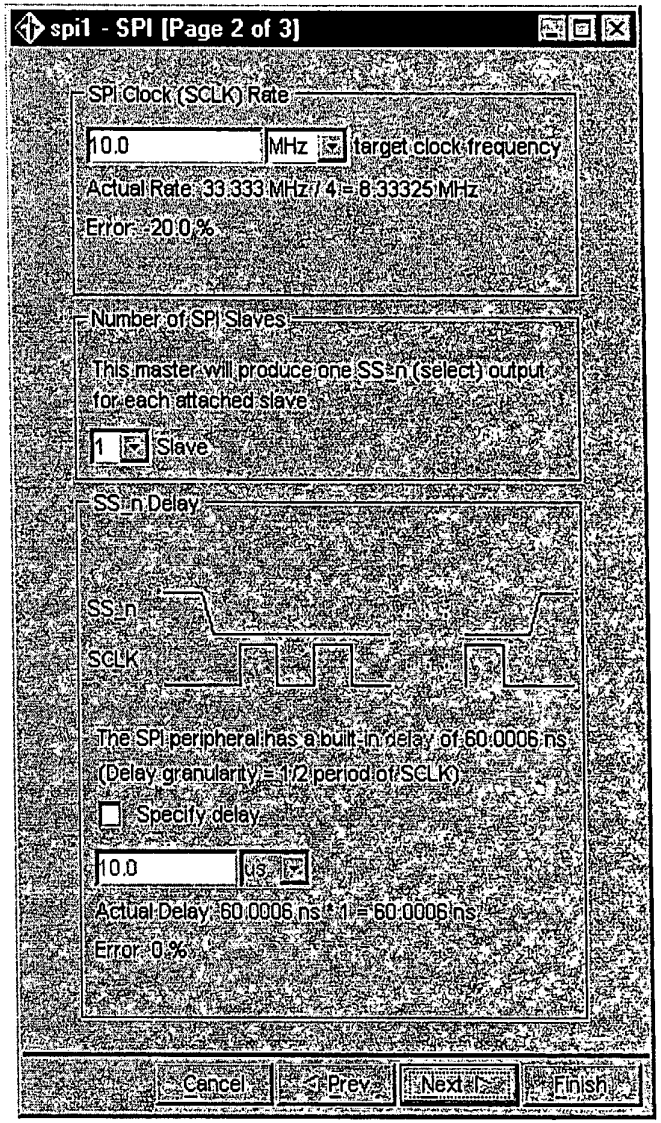


FIGURE 3P

FIGURE 3Q

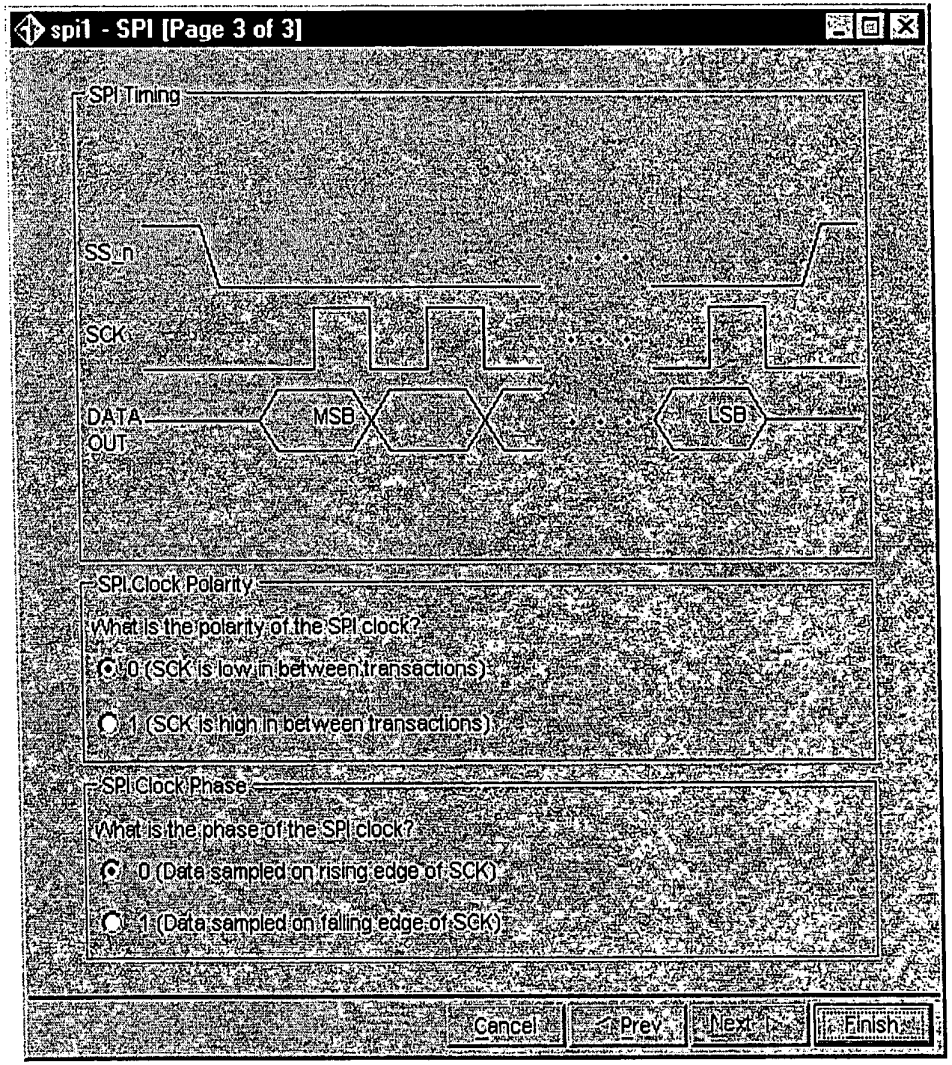

spi1 - SPI [Page 3 of 3]
SPI Timing
SS_n
SCK
DATA OUT
MSB
LSB
SPI Clock Polarity
What is the polarity of the SPI clock?
0 (SCK is low in between transactions)
1 (SCK is high in between transactions)
SPI Clock Phase
What is the phase of the SPI clock?
0 (Data sampled on rising edge of SCK)
1 (Data sampled on falling edge of SCK)
Cancel
< Prev
Next >
Finish

FIGURE 3R

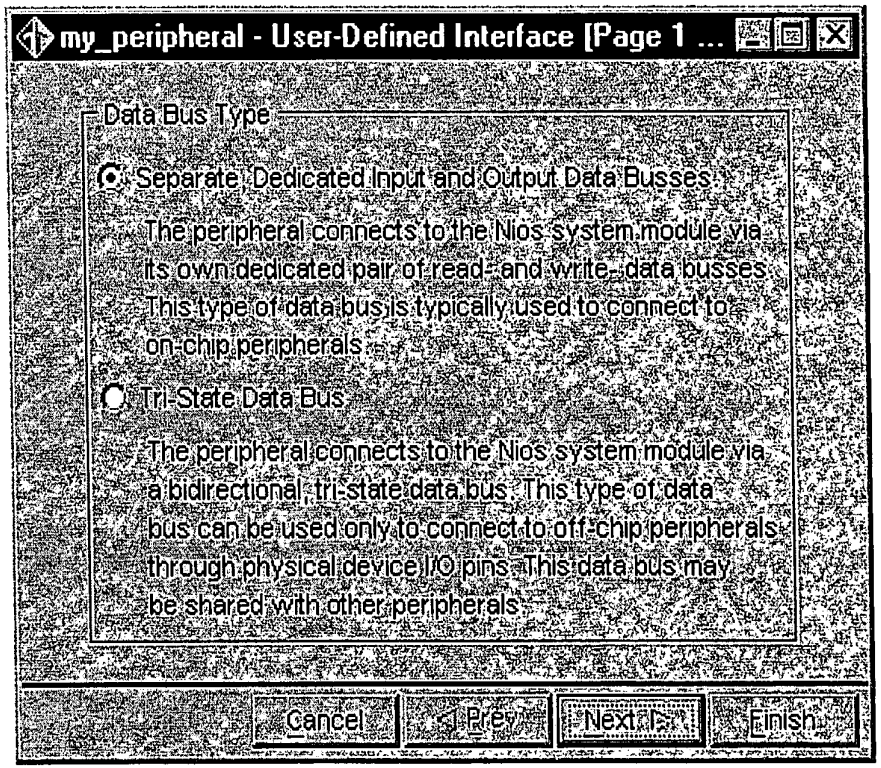


FIGURE 3S

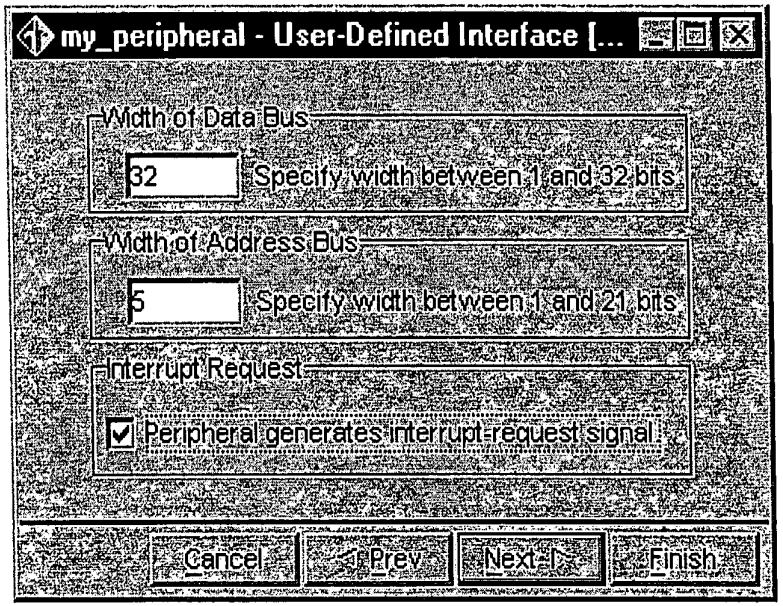

my_peripheral - User-Defined Interface [...
Width of Data Bus
32
Specify width between 1 and 32 bits
Width of Address Bus
5
Specify width between 1 and 21 bits
Interrupt Request
Peripheral generates interrupt request signal
Cancel
< Prev
Next >
Finish

FIGURE 3T

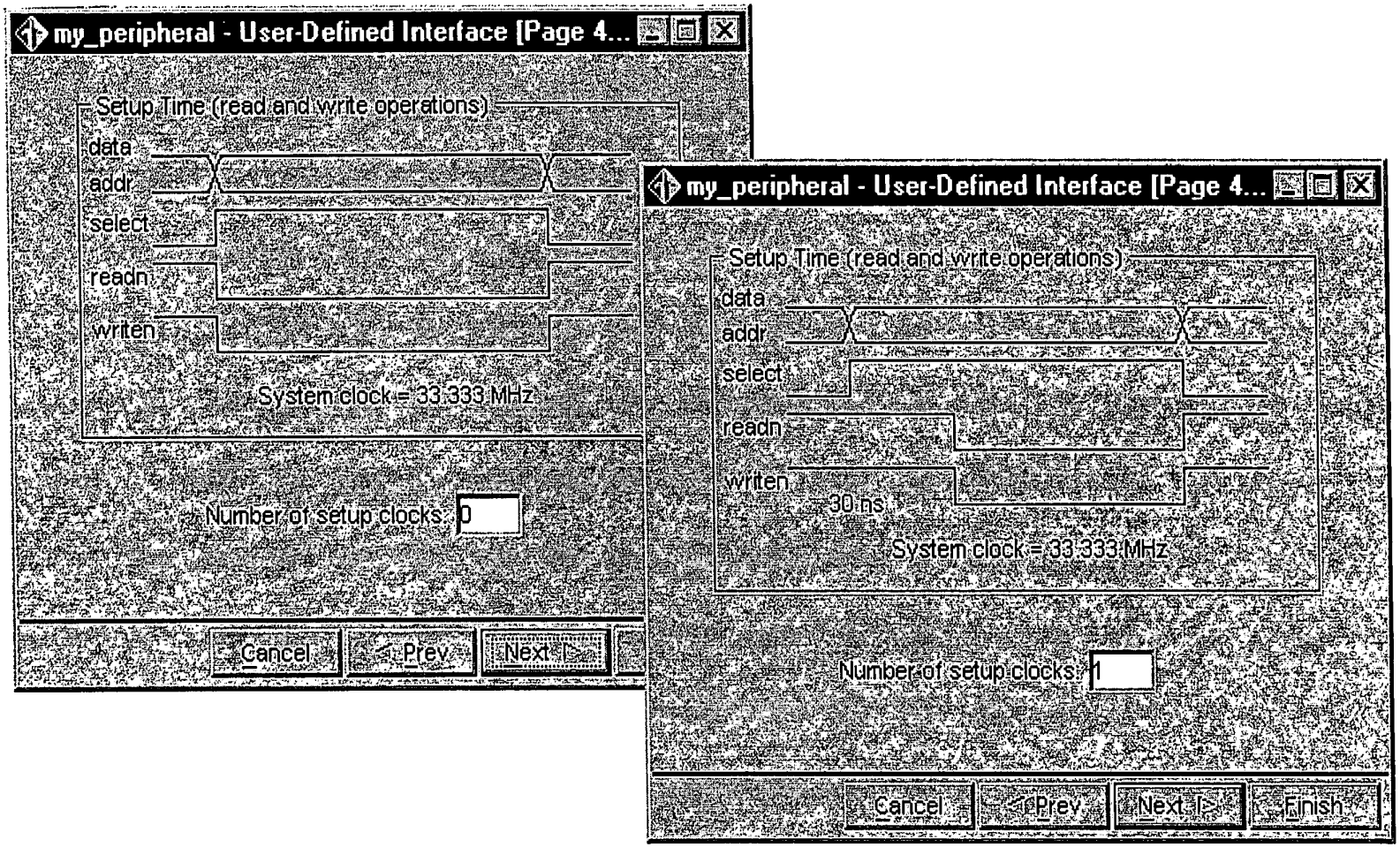

my_peripheral - User-Defined Interface [Page 4...
Setup Time (read and write operations)
data
addr
select
readn
writen
System clock = 33.333 MHz
Number of setup clocks: 0
Cancel
< Prev
Next >
my_peripheral - User-Defined Interface [Page 4...
Setup Time (read and write operations)
data
addr
select
readn
writen
30 ns
System clock = 33.333 MHz
Number of setup clocks: 1
Cancel
< Prev
Next >
Finish

FIGURE 3U

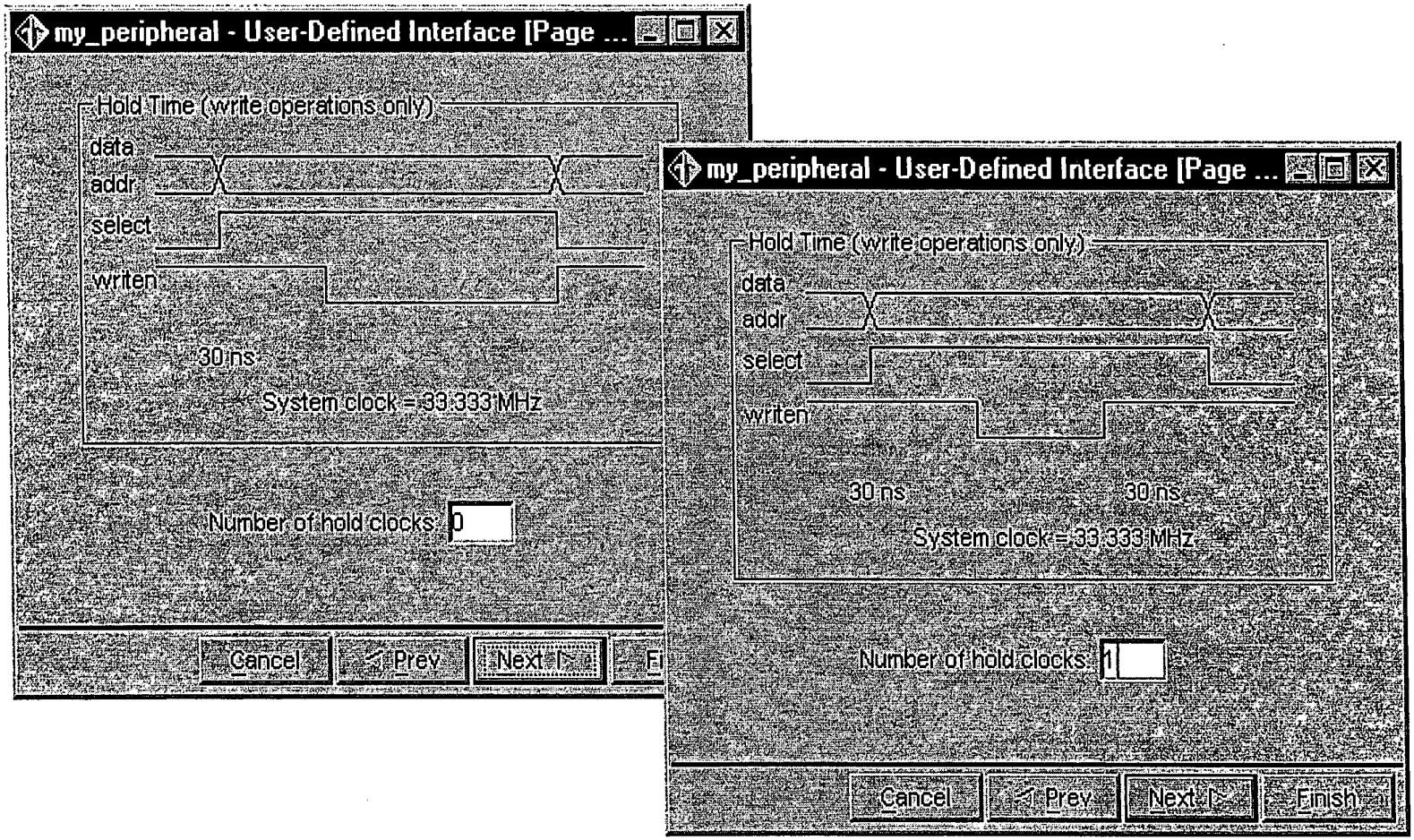


Figure 3V

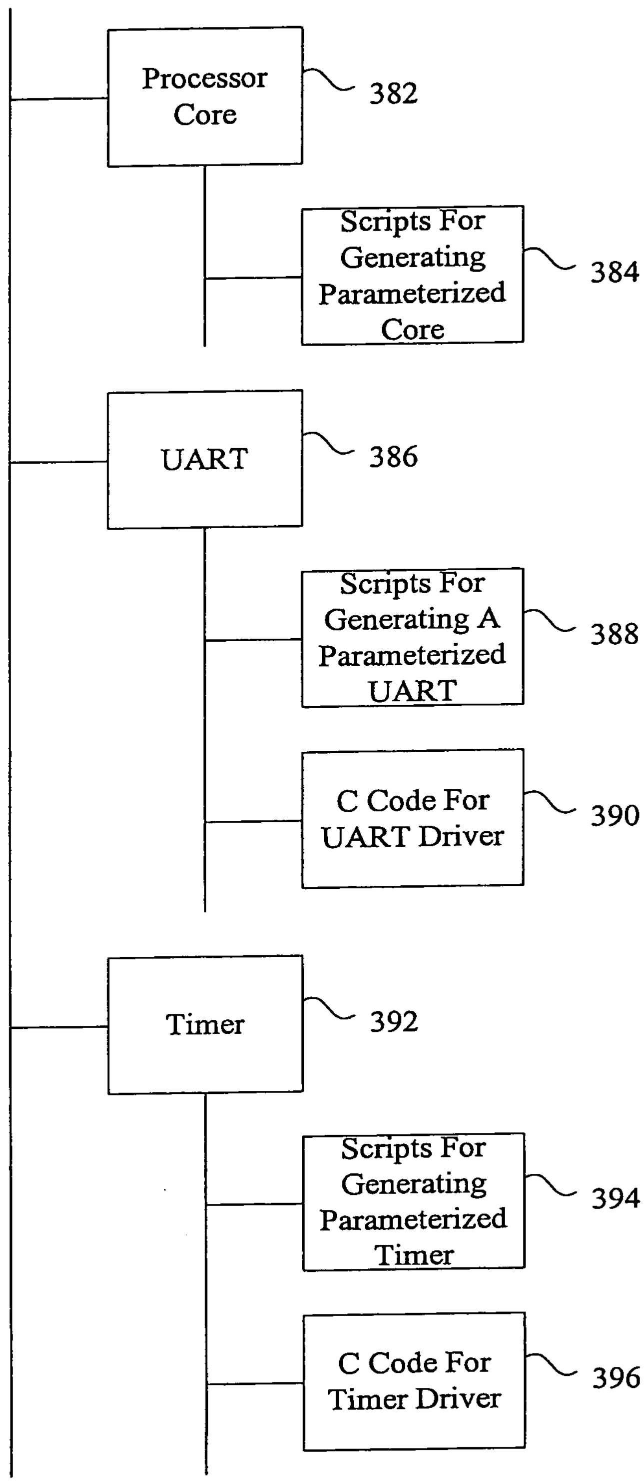


Figure 4

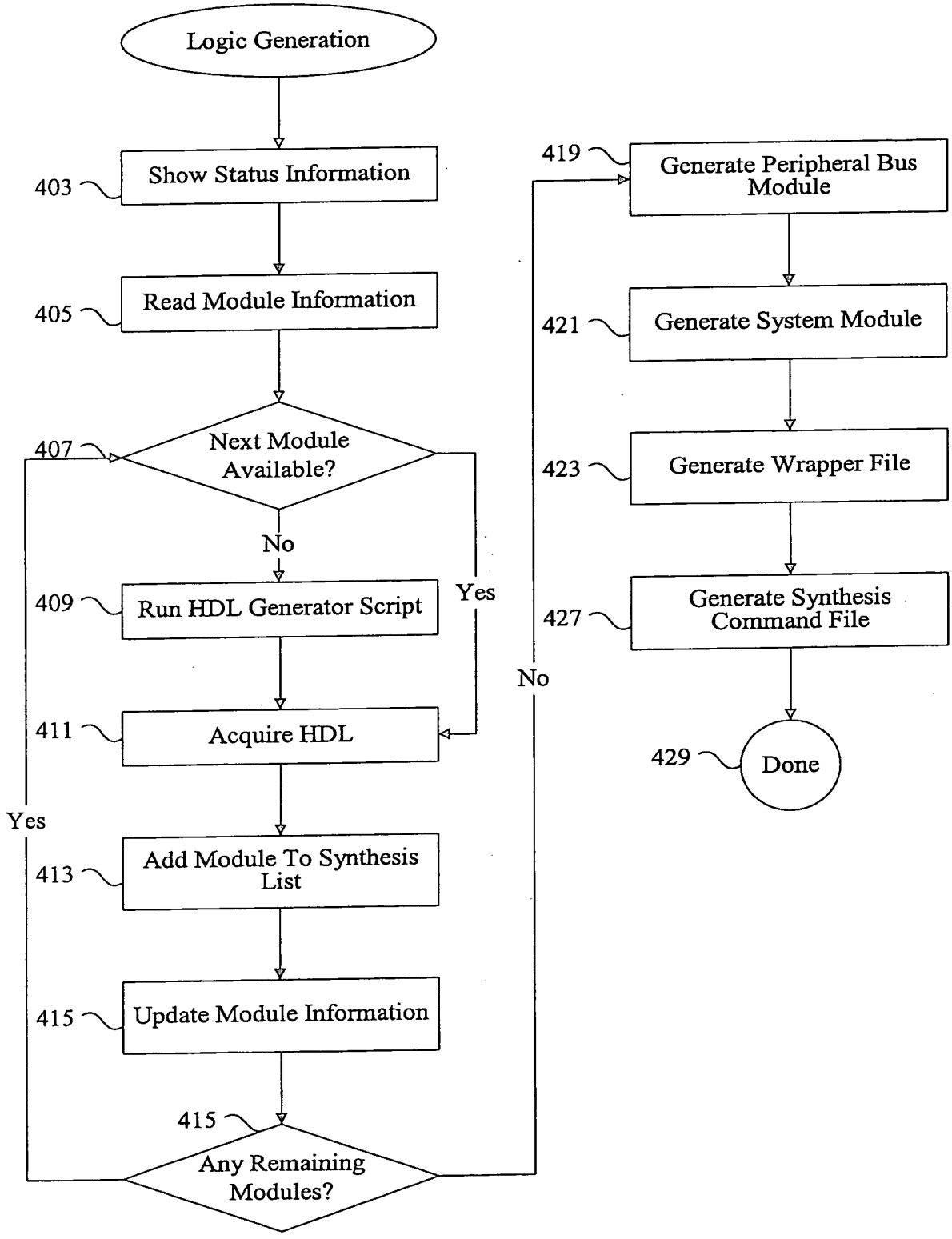

Logic Generation
403
Show Status Information
405
Read Module Information
407
Next Module Available?
No
Yes
409
Run HDL Generator Script
411
Acquire HDL
Yes
413
Add Module To Synthesis List
415
Update Module Information
415
Any Remaining Modules?
No
419
Generate Peripheral Bus Module
421
Generate System Module
423
Generate Wrapper File
427
Generate Synthesis Command File
429
Done

Figure 5

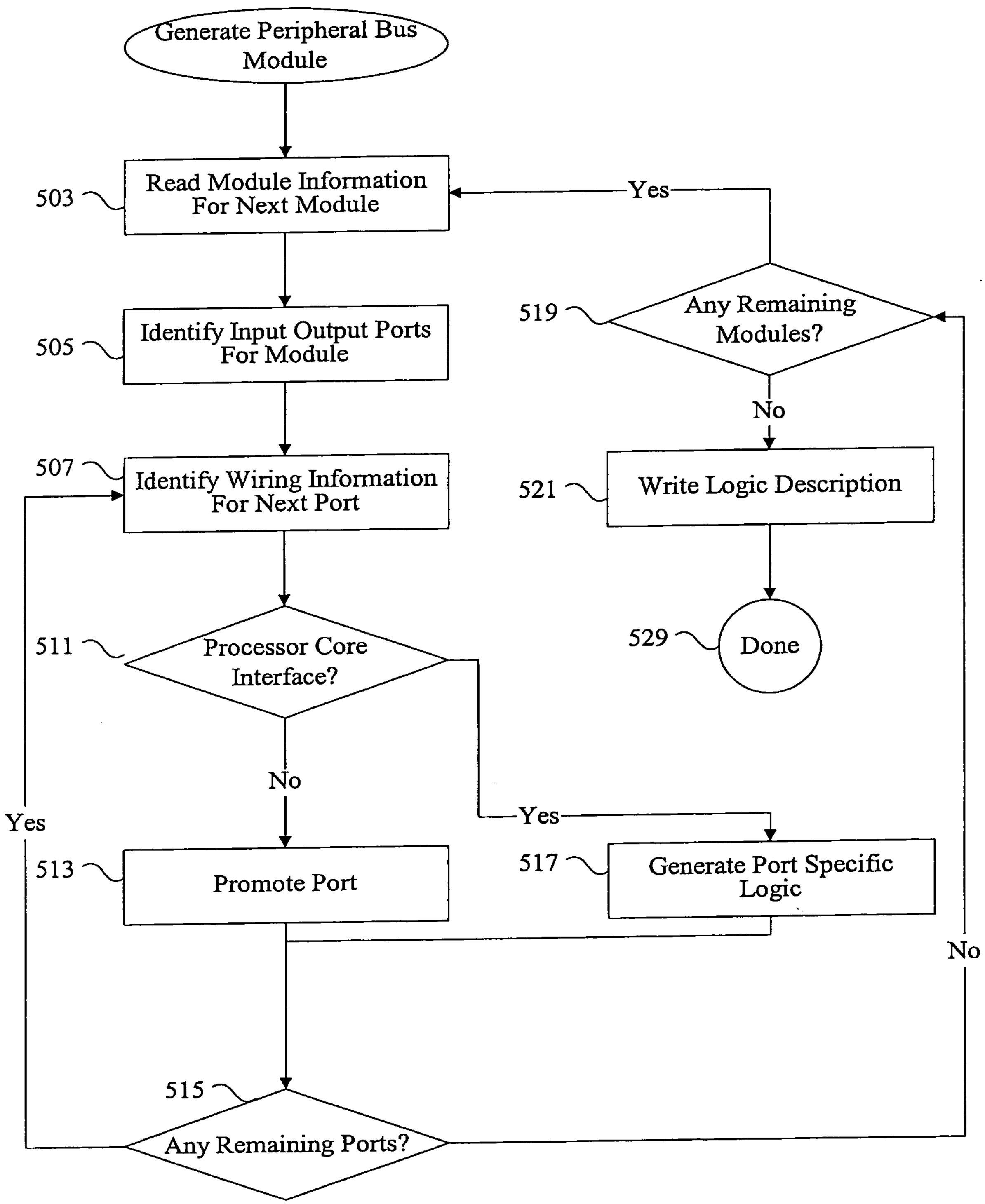


Figure 6A

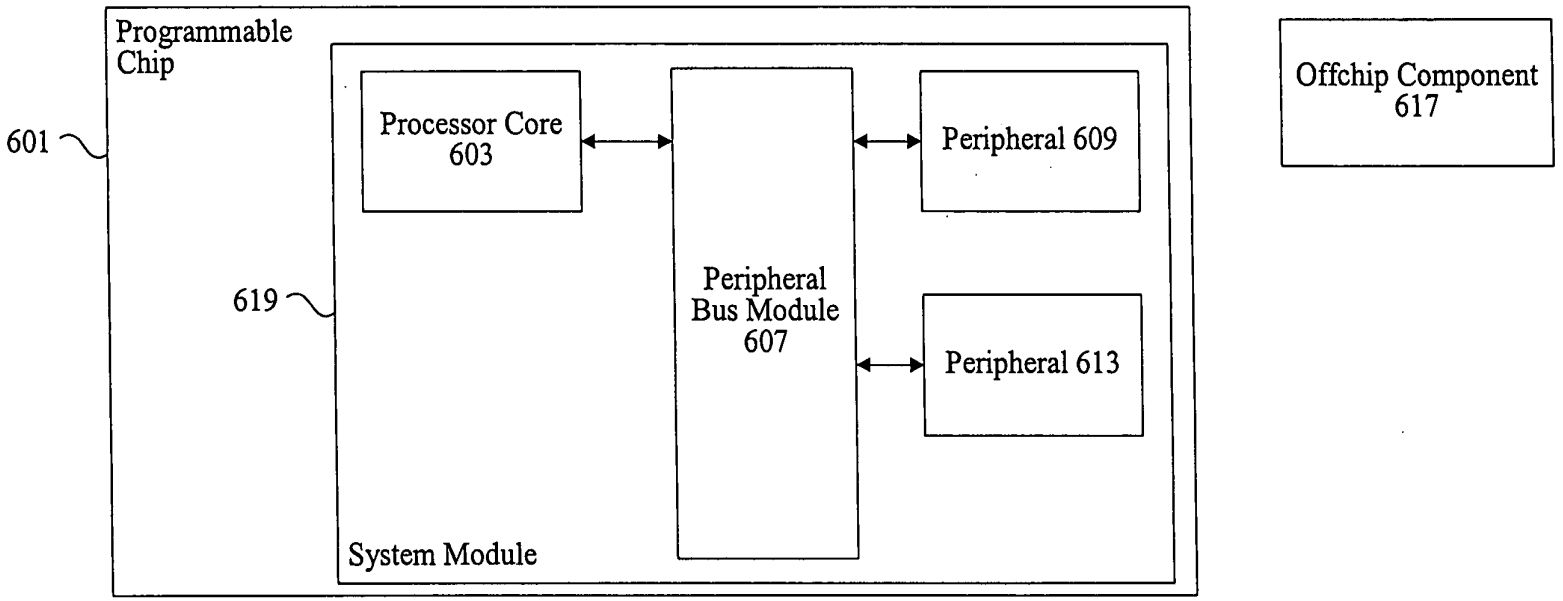

Programmable Chip
601
619
Processor Core 603
Peripheral Bus Module 607
Peripheral 609
Peripheral 613
System Module
Offchip Component 617

Figure 6B

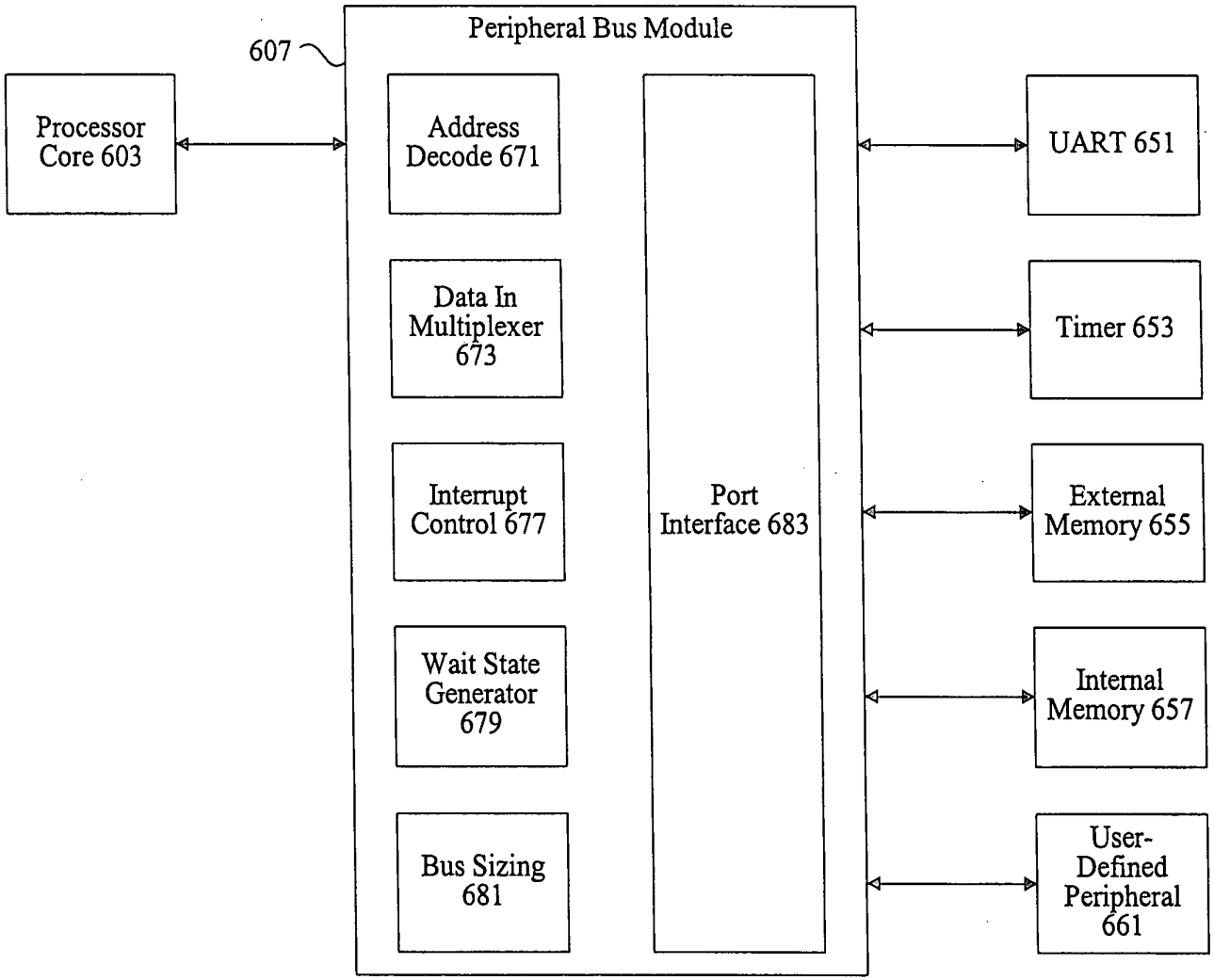

Peripheral Bus Module
607
Processor Core 603
Address Decode 671
Data In Multiplexer 673
Interrupt Control 677
Wait State Generator 679
Bus Sizing 681
Port Interface 683
UART 651
Timer 653
External Memory 655
Internal Memory 657
User-Defined Peripheral 661

FIGURE 7

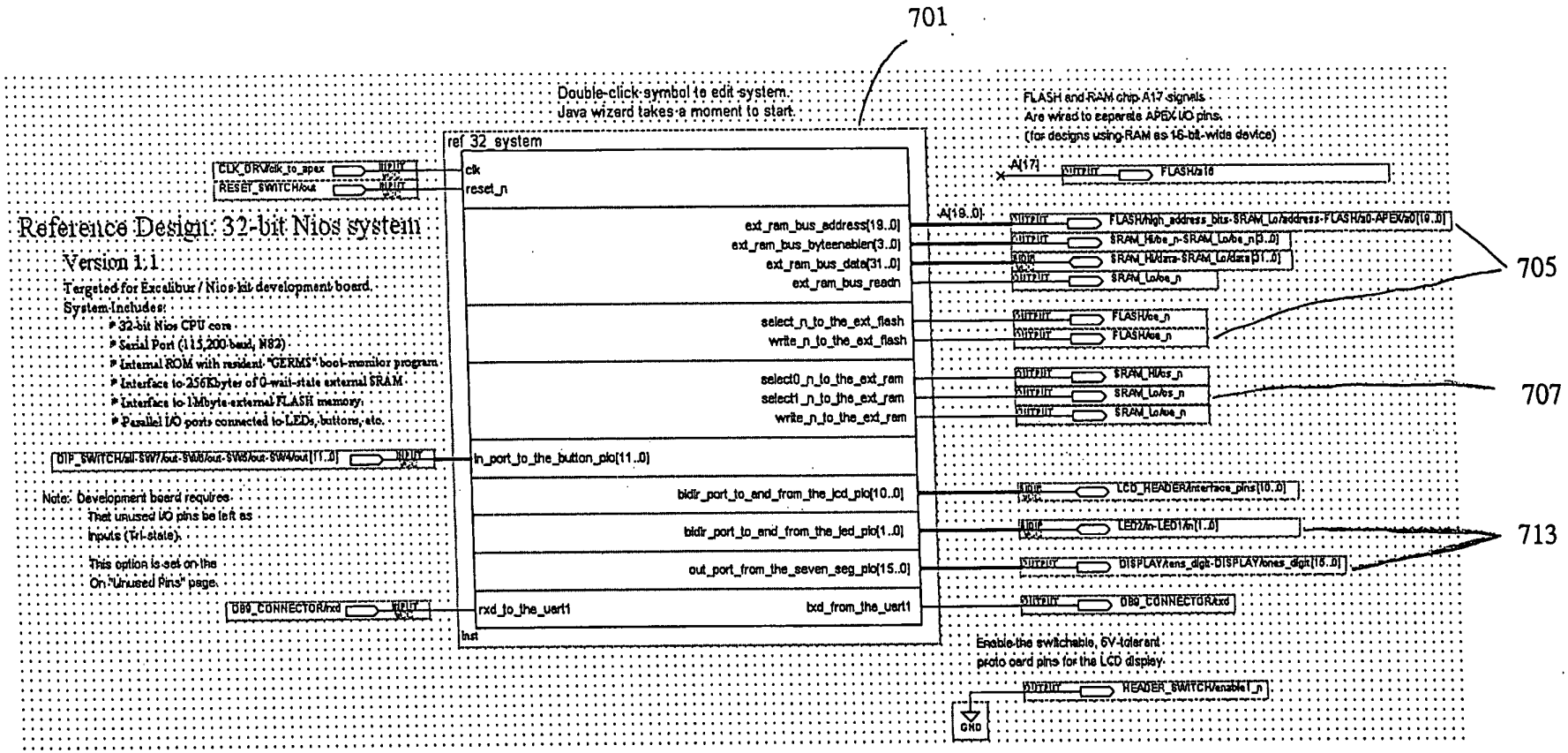
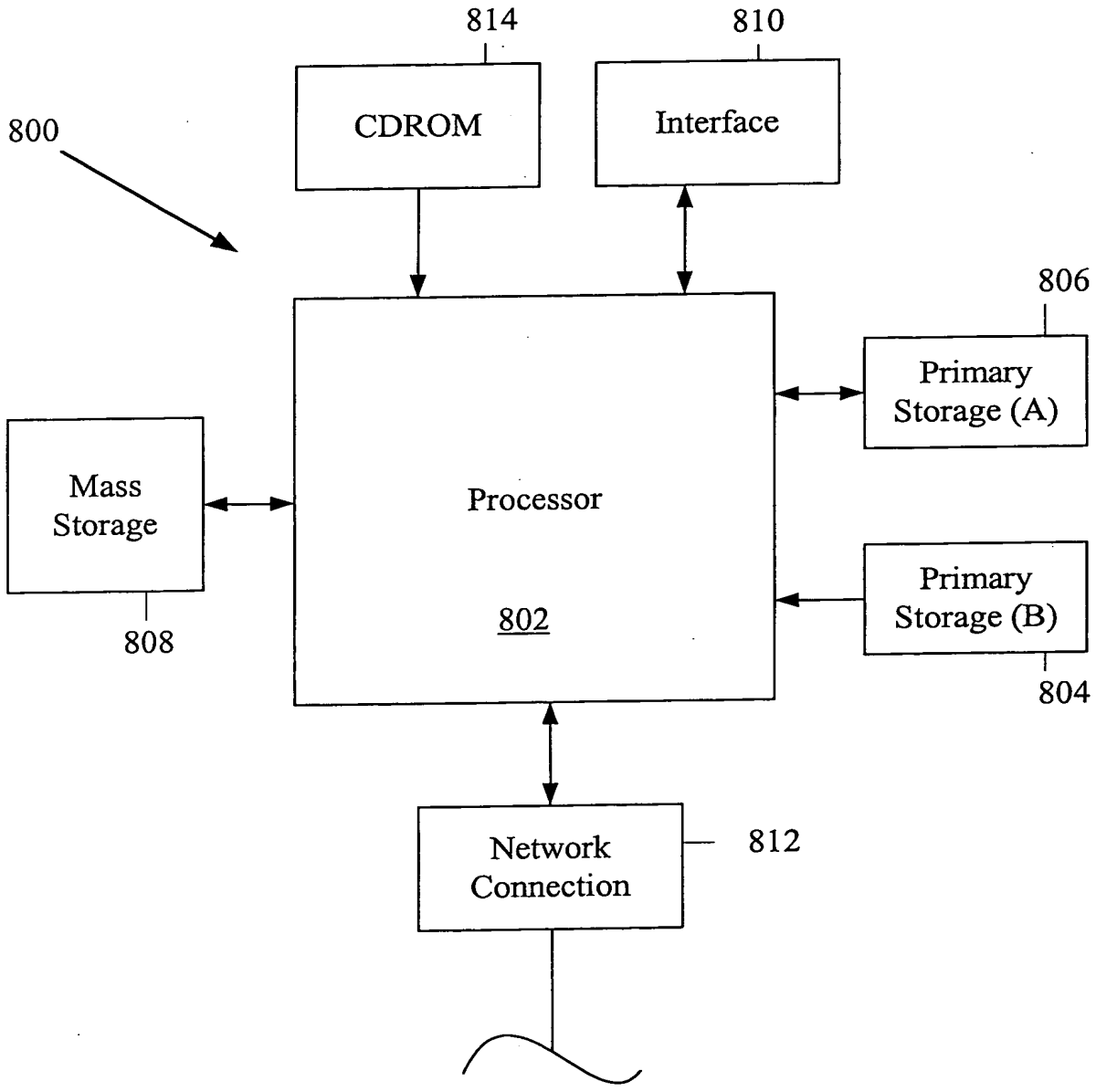

701
Double-click symbol to edit system.
Java wizard takes a moment to start.
ref_32_system
clk
reset_n
ext_ram_bus_address[19..0]
ext_ram_bus_byteenable[3..0]
ext_ram_bus_data[31..0]
ext_ram_bus_readn
select_n_to_the_ext_flash
write_n_to_the_ext_flash
select0_n_to_the_ext_ram
select1_n_to_the_ext_ram
write_n_to_the_ext_ram
in_port_to_the_button_pio[11..0]
bidir_port_to_and_from_the_lcd_pio[10..0]
bidir_port_to_and_from_the_led_pio[1..0]
out_port_from_the_seven_seg_pio[15..0]
rxd_to_the_uart1
txd_from_the_uart1
inst
CLK_OR/clk_to_apex
RESET_SWITCH/out
Reference Design: 32-bit Nios system
Version 1.1
Targeted for Excalibur / Nios kit development board.
System Includes:
32-bit Nios CPU core
Serial Port (115,200 baud, N82)
Internal ROM with resident "GERMS" boot-monitor program
Interface to 256Kbytes of 0-wait-state external SRAM
Interface to 1Mbyte external FLASH memory
Parallel I/O ports connected to LEDs, buttons, etc.
DIP_SWITCH/all_SW7out_SW6out_SW5out_SW4out[11..0]
Note: Development board requires
that unused I/O pins be left as
inputs (Tri-state).
This option is set on the
On "Unused Pins" page.
DB9_CONNECTOR/rxd
FLASH and RAM chip A17 signals
Are wired to seperate APEX I/O pins.
(for designs using RAM as 16-bit-wide device)
A[17]
FLASH/a16
A[19..0]
FLASH/high_address_bits-SRAM_Lo/address-FLASH/a0-APEX/a0[19..0]
SRAM_Hi/be_n-SRAM_Lo/be_n[3..0]
SRAM_Hi/data-SRAM_Lo/data[31..0]
SRAM_Lo/be_n
FLASH/oe_n
FLASH/we_n
SRAM_Hi/cs_n
SRAM_Lo/cs_n
SRAM_Lo/we_n
LCD_HEADER/interface_pins[10..0]
LED2/n-LED1/n[1..0]
DISPLAY/tens_digit-DISPLAY/ones_digit[15..0]
DB9_CONNECTOR/txd
Enable the switchable, 5V-tolerant
proto card pins for the LCD display.
HEADER_SWITCH/enable_n
GND
705
707
713

Figure 8


814
810
CDROM
Interface
800
806
Primary Storage (A)
Mass Storage
Processor
802
Primary Storage (B)
808
804
Network Connection
812